Amendments to the Claims:

Please cancel claims 1-36, leaving claims 37-49 for examination.

Listing of Claims:

1-36. (Cancelled)

37. (Original) A method for forming a semiconductor structure on a surface of a substrate, comprising:

forming an active region in the substrate;

forming an epitaxial post on the substrate over the active region, the epitaxial post having at least one surface extending outwardly from the surface of the substrate and further having a surface opposite of the surface of the substrate;

forming a gate structure adjacent to at least a portion of all the outwardly extending surface of the epitaxial post; and

forming a capacitor on the exposed surface of the epitaxial post.

38. (Original) The method of claim 37 wherein forming the epitaxial post comprises:

forming first and second sacrificial structures spaced laterally apart on the substrate;

forming sidewalls on the first and second sacrificial structures to define a trench region therebetween, the surface of the substrate exposed in the trench region;

forming an epitaxial layer on the exposed surface of the substrate in the trench region.

39. (Original) The method of claim 38 wherein forming the gate structure comprises:

removing the sidewalls on the first and second sacrificial structures to define a gap between the sacrificial structures and the epitaxial post;

forming a gate oxide over exposed surfaces of the epitaxial post;

depositing polycrystalline silicon in the gap region;

recessing the polycrystalline silicon below an upper surface of the epitaxial post; and

forming an insulating region on the polycrystalline silicon in the gap between the polycrystalline silicon and the upper surface of the epitaxial post.

40. (Original) The method of claim 37 wherein forming the capacitor comprises:

forming a first layer of doped polycrystalline silicon on the surface opposite of the surface of the surface of the substrate of the epitaxial post;

diffusing dopants from the first layer of doped polycrystalline silicon to the epitaxial post;

forming a capacitor dielectric layer over the first layer of doped polycrystalline silicon; and

forming a second layer of doped polycrystalline silicon on the capacitor dielectric layer.

41. (Original) The method of claim 37, further comprising:

depositing an insulating interlayer over the gate structure;

opening a via through the insulating interlayer to expose a portion of the active region; and

depositing a conductive material over the insulating interlayer and into the opening to contact the exposed portion of the active region.

42. (Original) The method of claim 37 wherein forming the active region comprises forming buried digit lines in the substrate.

43. (Original) A method for forming pair of memory cells on a surface of the substrate, comprising:

forming an active region in the substrate;

forming a vertical transistor in an epitaxial post formed on the substrate surface and extending from the surface of the substrate, the vertical transistor further having a gate formed around a perimeter of the epitaxial post; and

forming a capacitor on the vertical transistor.

44. (Original) The method of claim 43 wherein forming the vertical transistor comprises:

forming a gate oxide on a surface defining the perimeter of the epitaxial post;

forming a gate on the gate oxide; and

forming insulating sidewalls on the gate.

45. (Original) The method of claim 43 wherein the forming the capacitor comprises forming a container shaped capacitor structure.

46. (Original) The method of claim 43, further comprising forming a diffusion region in the epitaxial post adjacent the capacitor.

47. (Original) The method of claim 43 wherein forming the active region comprises forming a buried digit line.

48. (Original) The method of claim 43, further comprising forming a digit line contact over the active region and proximate the vertical transistor.

49. (Original) The method of claim 43, further comprising forming an insulating region around the perimeter of the epitaxial post, and interposed between the capacitor and the vertical transistor.